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Windows Home Server

MS-7436 (MS-6631)

Version 1.0

CPU:

Intel Dimondville

System Chipset:

Intel 945GC (North Bridge)

Intel ICH7(South Bridge)

On Board Chipset:

BIOS -- SPI

LAN -- Realtek RTL8111C

Clock Generator - ICS954119

Main Memory:

DDR II SO-DIMM x 1 (Max 2GB)

CF Card Connector for flash Memory

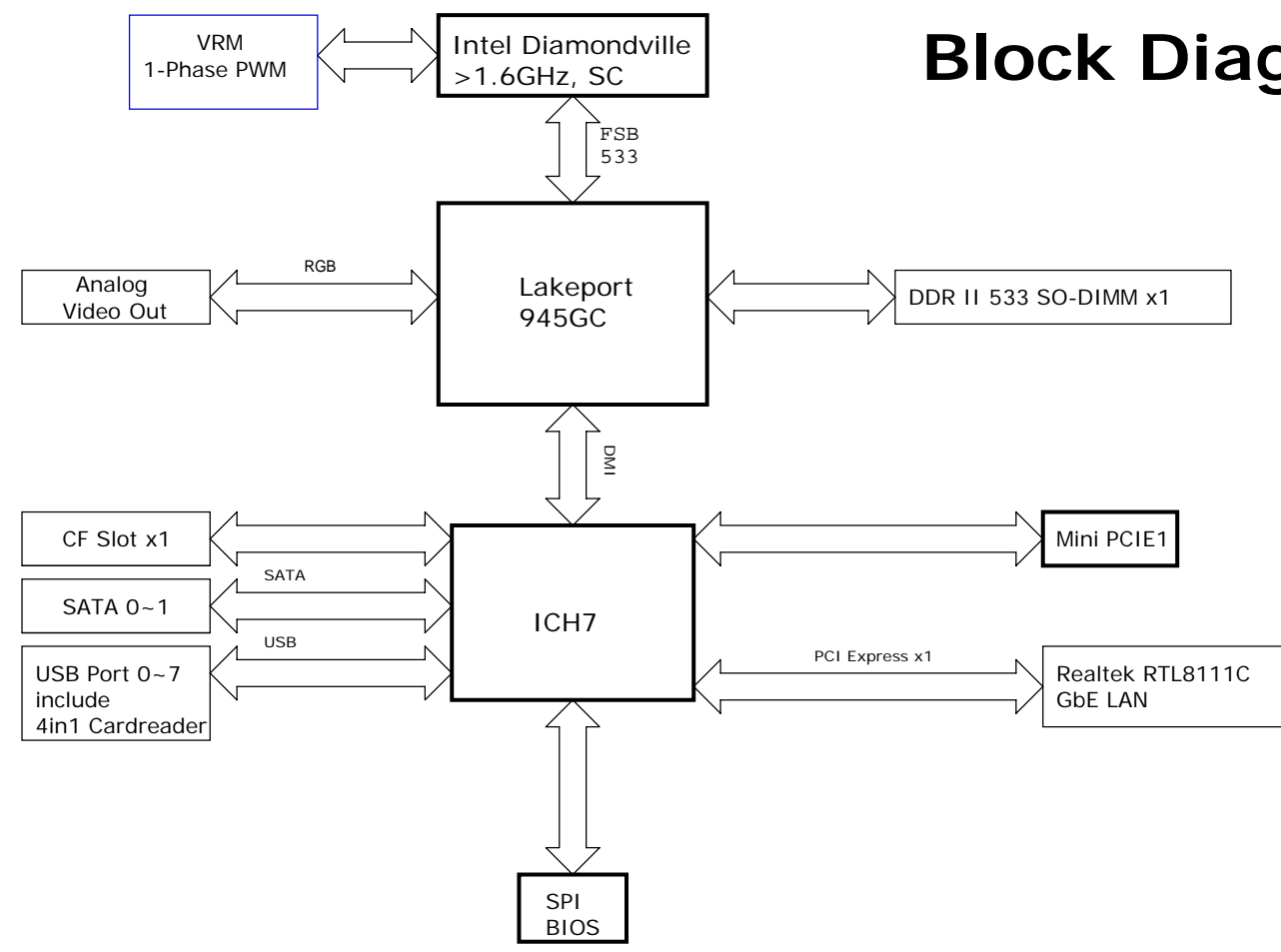
Expansion Slots:

Internal Mini PCIE x1

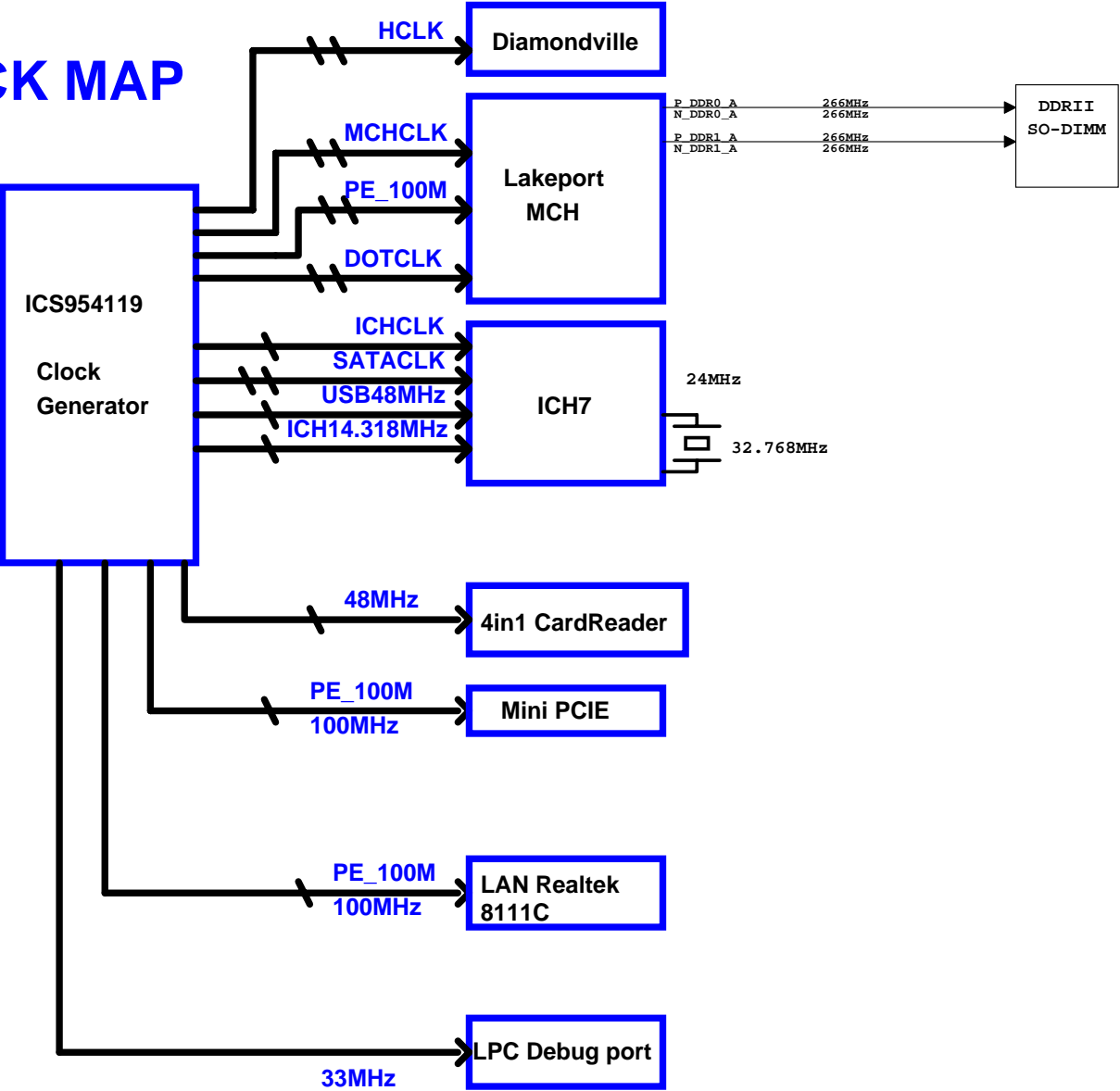
Intersil PWM:

Controller: 6314

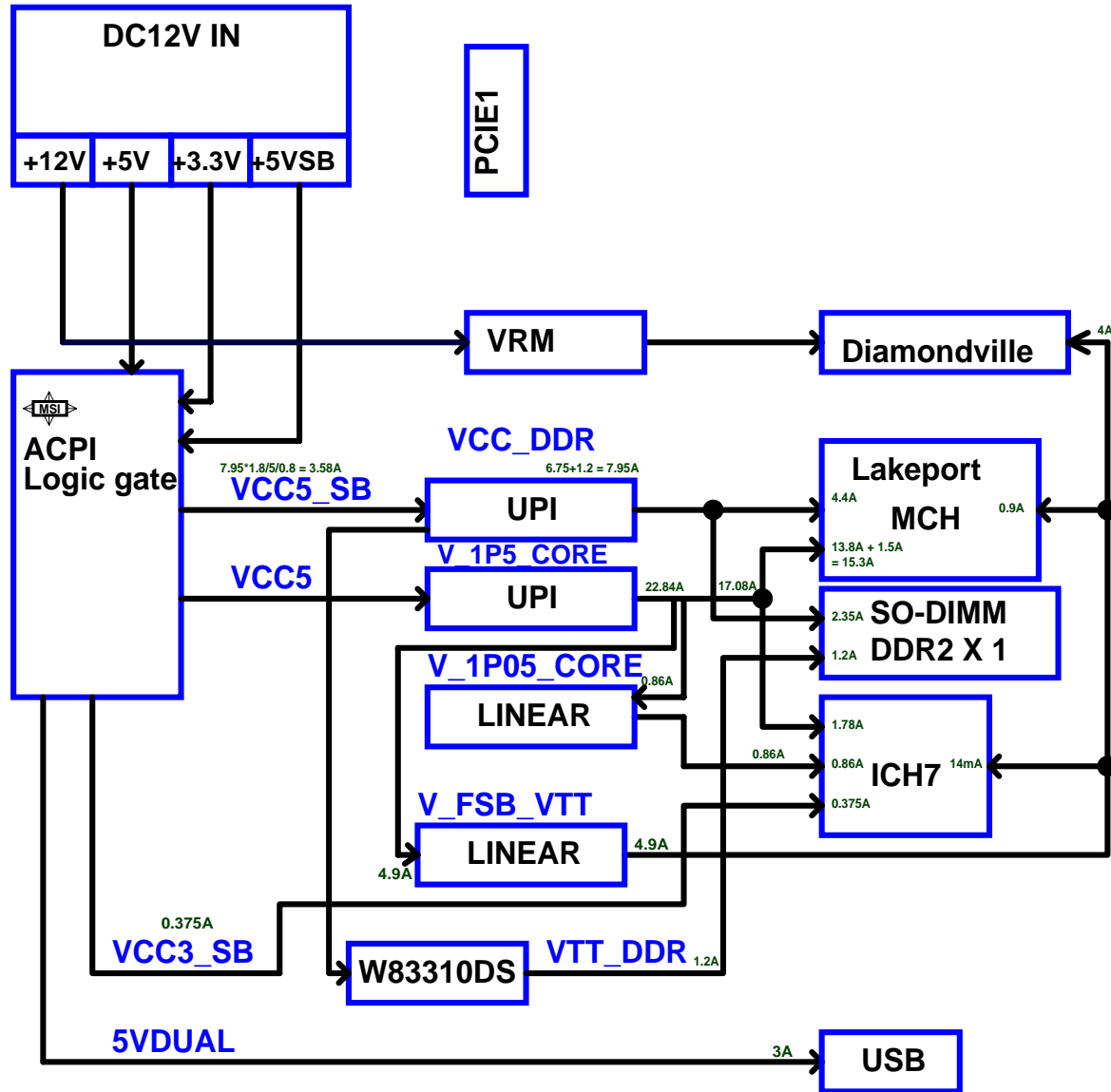
Block Diagram



CLOCK MAP



POWER MAP



ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name or status
GPIO[0]	SIO_SMI#	AB18	I/O	Vcc3p3	N	Y	5	Input	pull high VCC3
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQE#
GPIO[3]	PIRF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	ATADET0	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	GPI7	AC18	I/O	Vcc3p3	N	Y	3.3	Input	pull high VCC3
GPIO[8]	SIO_PME#	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME# pull high VCC3_SB
GPIO[9]	WLAN_PWRON	E20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[12]	HDD1_LED_mount	F19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[13]	HDD2_LED_FAIL	E19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[14]	ADT7467_ALERT	R4	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[15]	Bios_recovery#	E22	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[24]	HDD1_LED_mount	R3	I/O	VccSus3p3	N	N	3.3	NO CHANGE	NC
GPIO[25]	S1_3_LED	D20	I/O	VccSus3p3	Y	N	3.3	1	NC
GPIO[26]	HDD2_LED_mount	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	SUSPEND_LED	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	HDD1_LED_FAIL	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#2	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#5
GPIO[30]	OC#2	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#6
GPIO[31]	OC#2	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#7
GPIO[32]	CLEAR_CMOS#	AG18	I/O	Vcc3p3	N	N	3.3	1	CLEAR_CMOS#, ONLY pull high VCC3
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	GNT4#
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD
GPI[15..0] can configured to cause a SMI# or SCI.									

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39;36;23;21;19;7;0]: default as inputs and should be pulled up to Vcc3.3 if unused.
GPIO[31;29;15;8]: default as inputs and should be pulled up to VccSus3.3 if unused.

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these				
GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-down
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

SIGNAL	DEVICE
MiniPCleRST#	MINI PCIE SLOT
TPMRST#	TPM
LANRST#	LAN 8111C
PCIRST_ICH7#	BUFFER IC
CF_RST#	CF_CARD
H_CPURST#	CPU
FWHRST#	LPT Debug port
MCHRST#	MCH

SMBCLK, SMBDATA, DDR2, PCIEX1, CLKGEN, ICH7, ADT7464

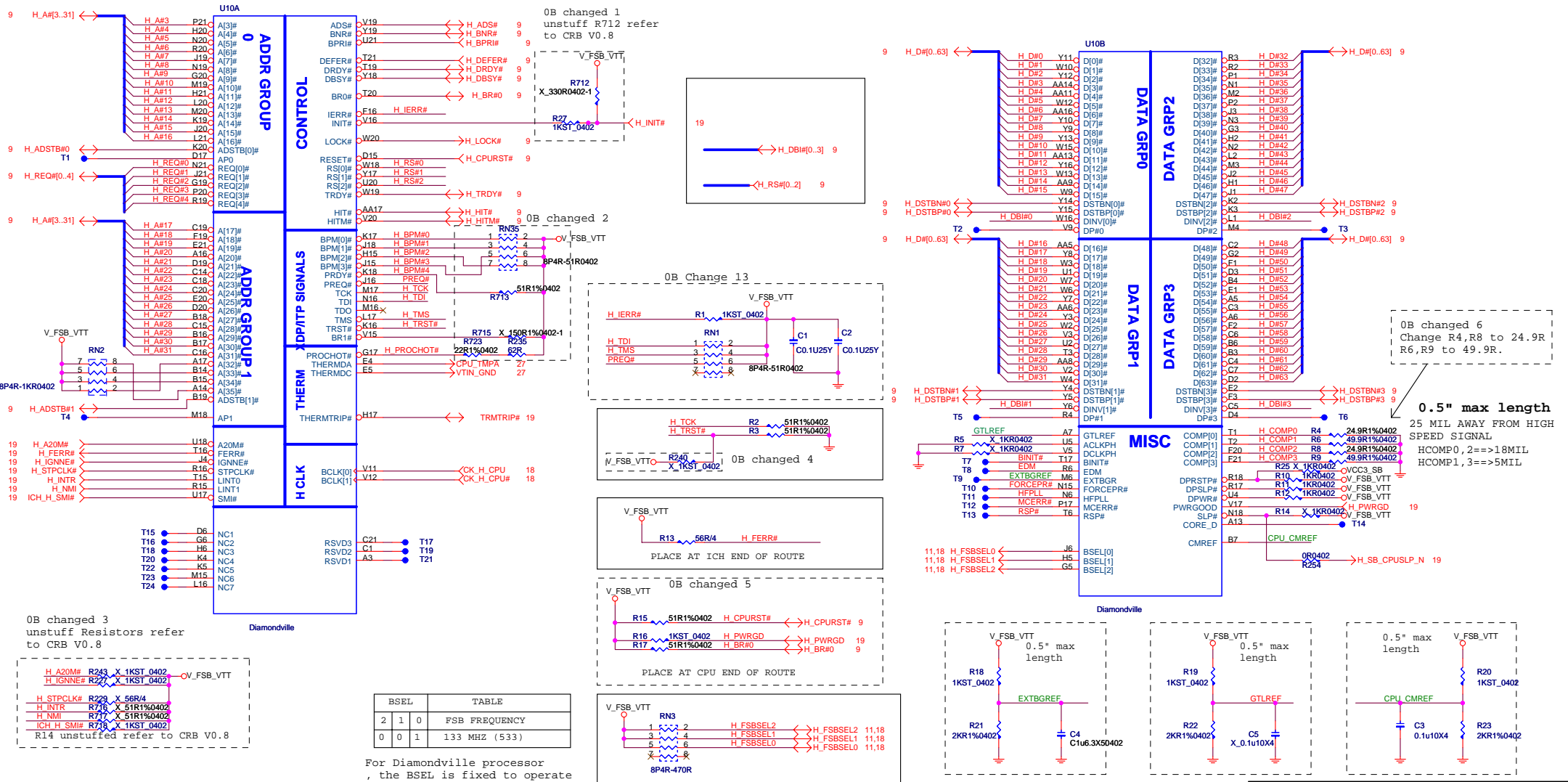
DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2

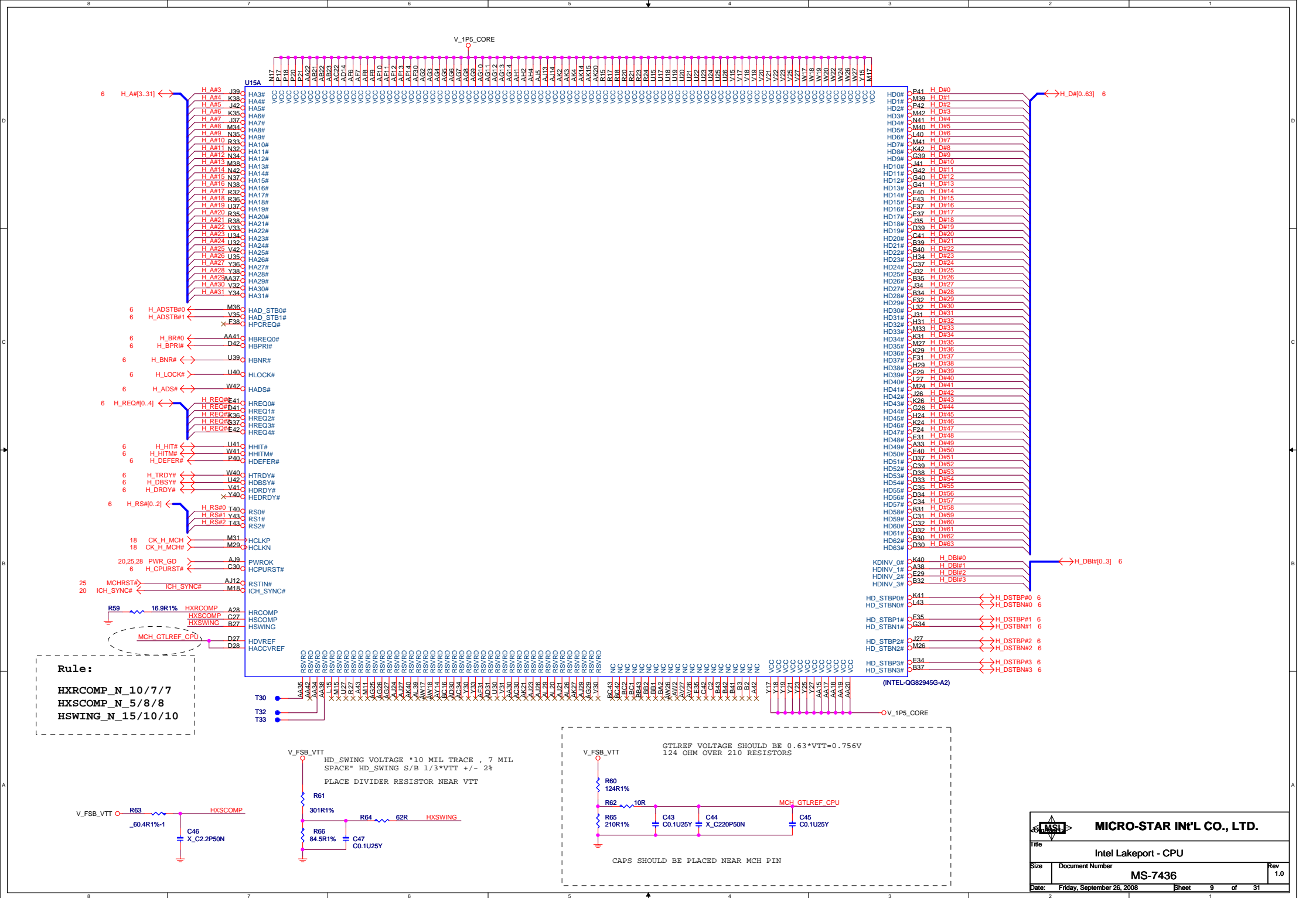
JUMPER SETTING

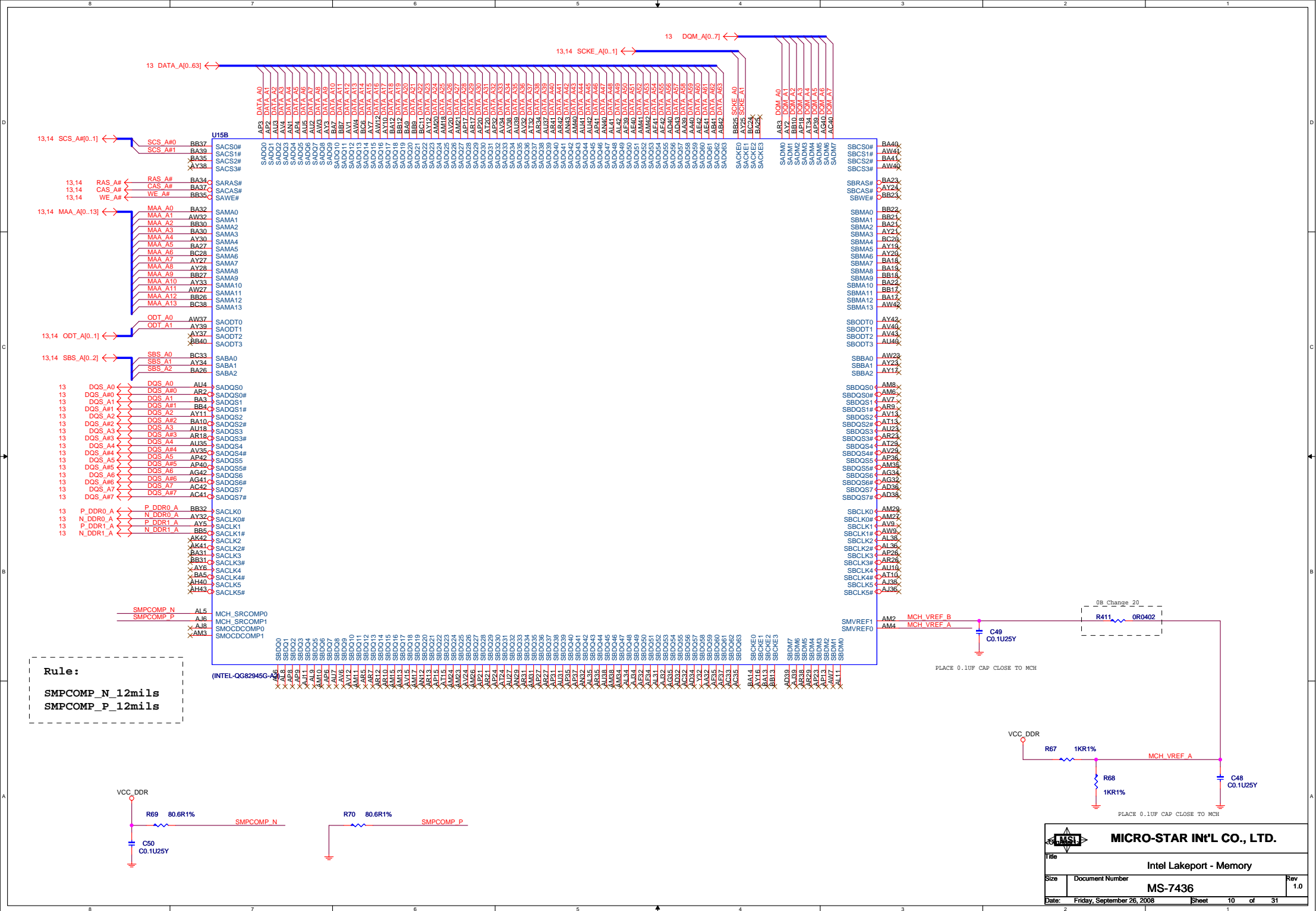
JBAT1	(1-2)NORMAL	(2-3)CLEAR
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CPU SIGNAL BLOCK

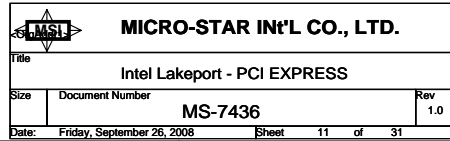


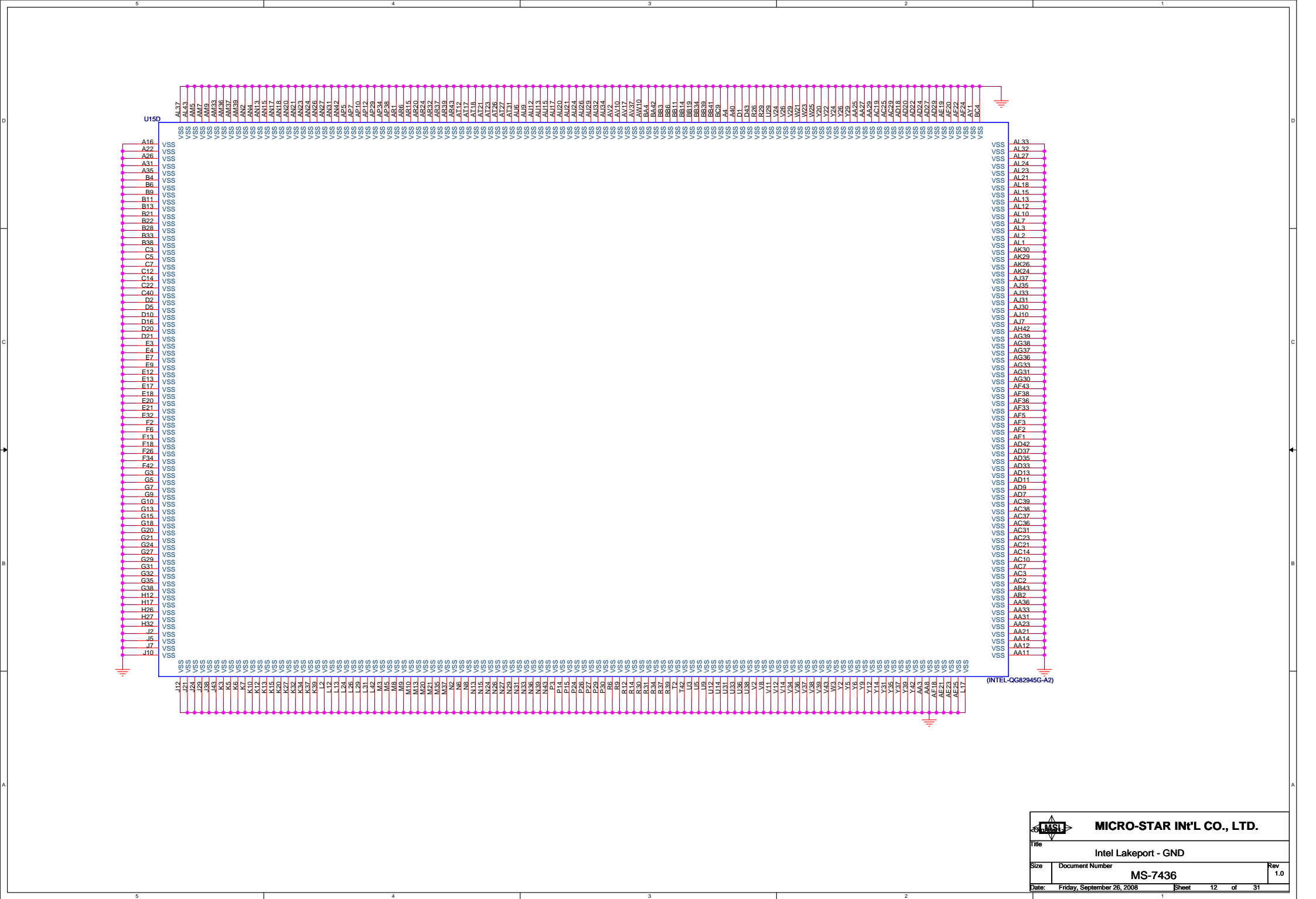
For Diamondville processor
, the BSEL is fixed to operate
at 133-MHz BCLK frequency.



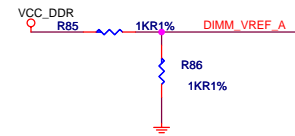
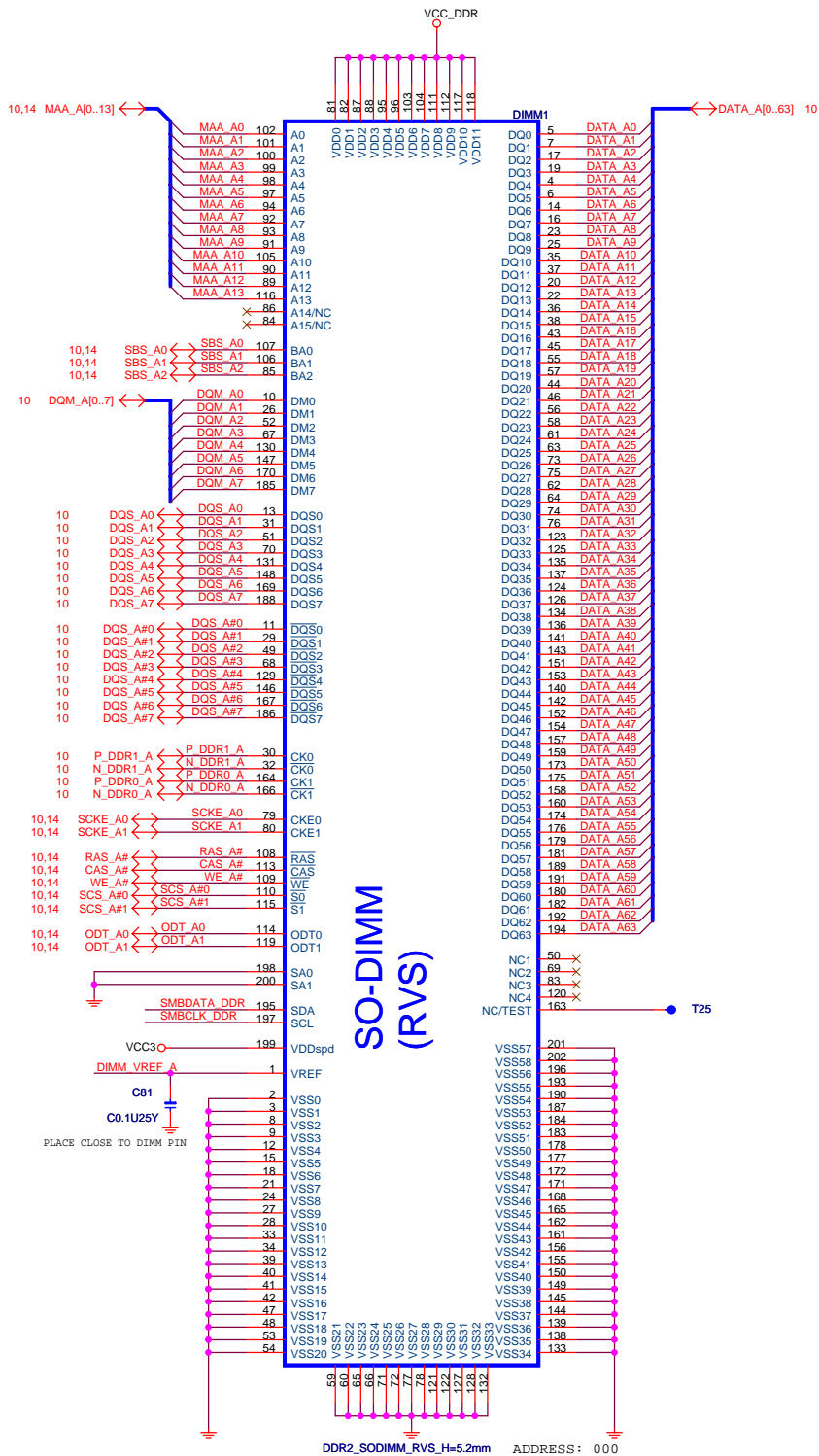


```
0: Only SDVO or PCI-E Operational
1: SDVO and PCI-E operating
simultaneously via PCI Express-G
port
```



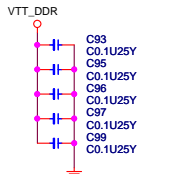
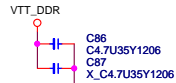


DDR2 SO-DIMM

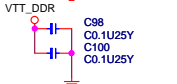
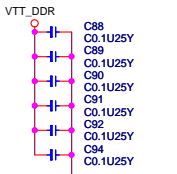
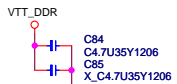


MICRO-STAR INT'L CO., LTD.	
Title: DDR II SO-DIMM	
Size: Document Number	MS-7436
Date: Friday, September 26, 2008 Sheet 13 of 31	

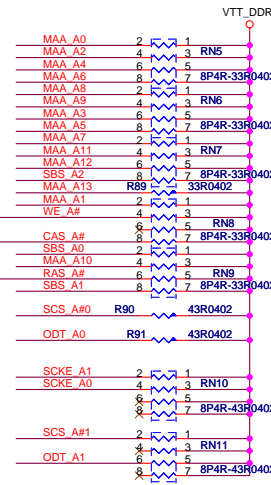
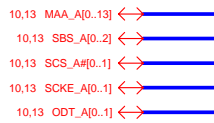
CHANNEL A V_SM_VTT
DECOUPLING CAPS



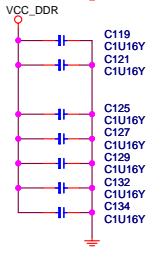
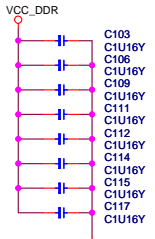
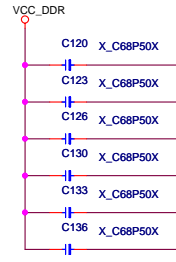
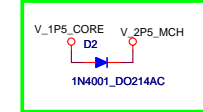
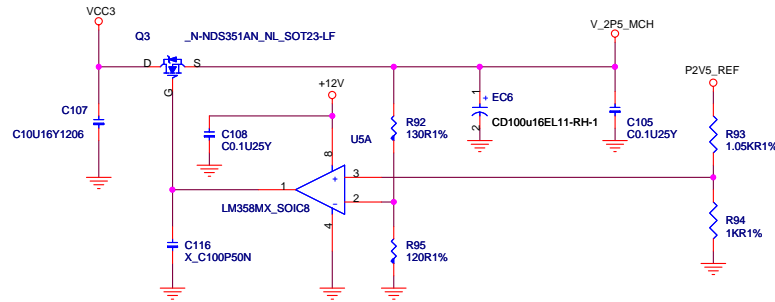
CHANNEL B V_SM_VTT
DECOUPLING CAPS

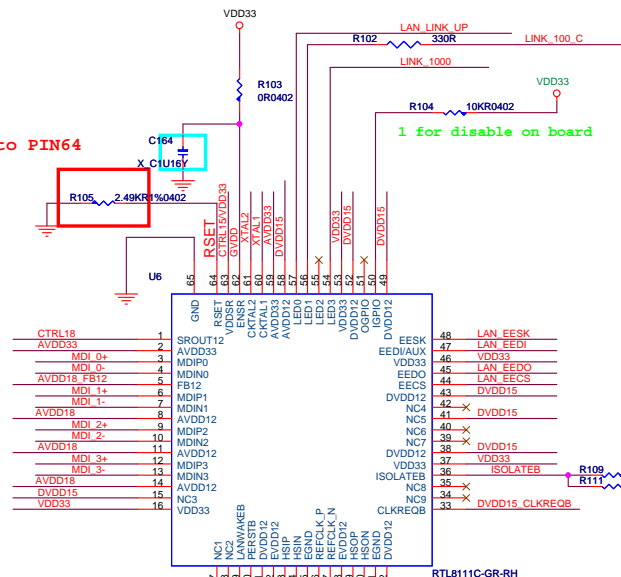


SCS_A#0 change 43 ohm



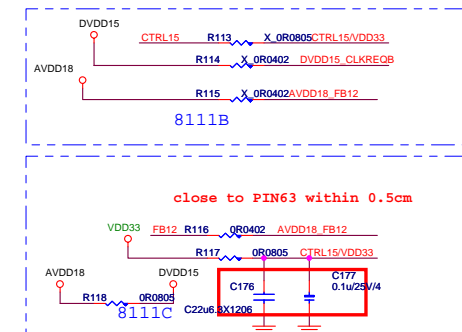
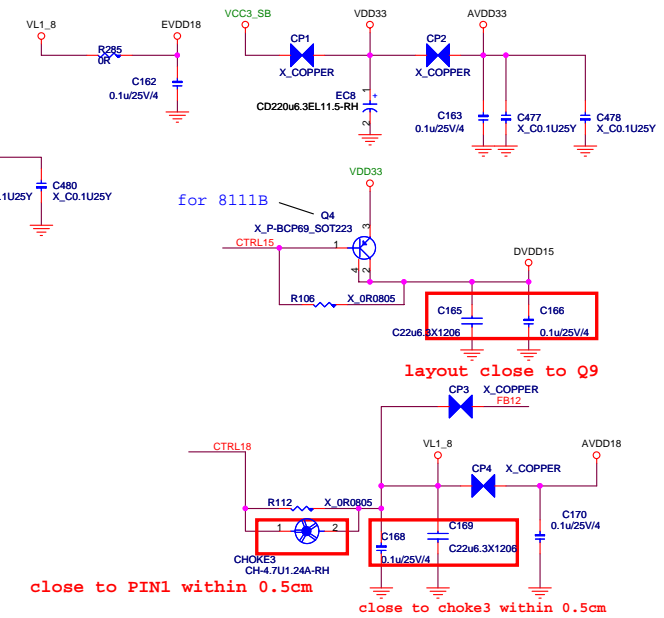
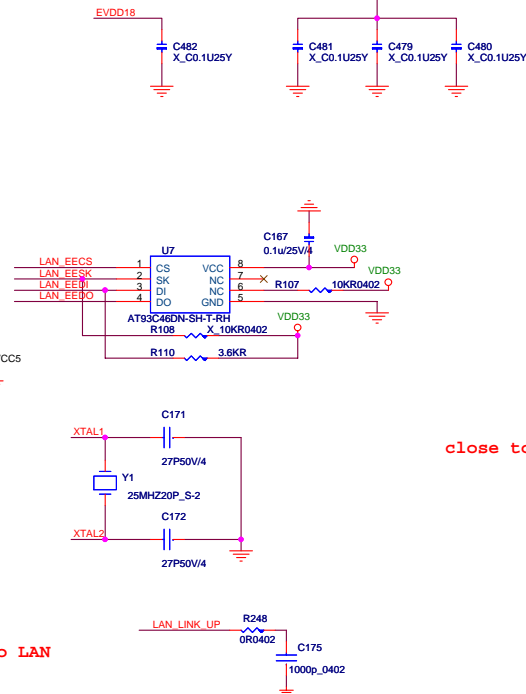
Grantsdale GMCH Power Sequencing
Requirement Between 1.5V Core and 2.5V DAC







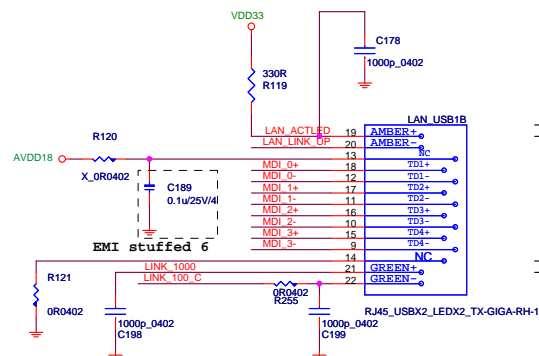
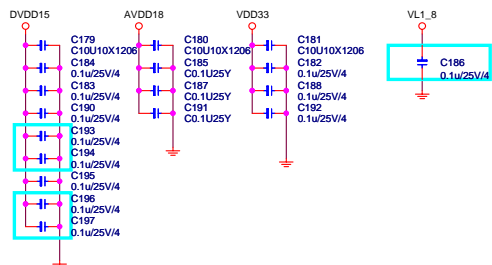


	RTL8111B / RTL8101E	RTL8111C	
AVDD33	3.3V	3.3V	
AVDD18	1.8V	1.2V	
EVDD18	1.8V	1.2V	
DVDD15	1.5V	1.2V	

	Q9	Q10
RTL8111B	<i>Need</i>	<i>Need</i>
RTL8111C	<i>N/A</i>	<i>N/A</i>

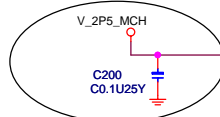


Power consumption			Giga-Lan		10/100-Lan	
	1G	100M	N58-22F0181-S42		N58-22F0061-S42 N58-22F0061-F02	
3.3V	103mA	TBD	Link	Yellow	Link	Yellow
1.5V	367mA	TBD	Active	Blinking	Active	Blinking
1.8V	198mA	TBD	1000	Orange	100	Green
			100	Green	10	None
			10	None		
			19		19	
			20	Yellow	20	Yellow
			21	Orange	21	
			22		22	
				Green		Green



Video Connector

Power 20 mils



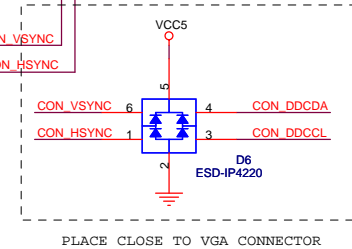
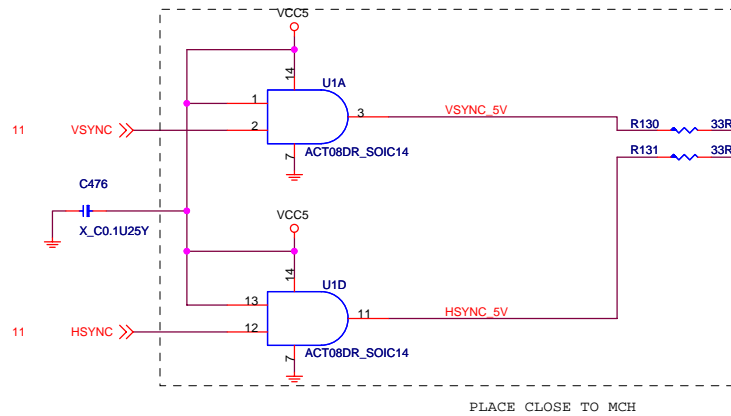
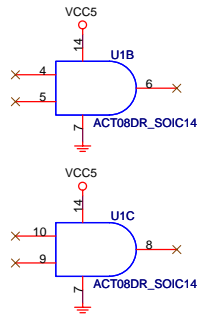
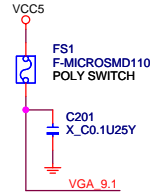
After 150 ohm

5 mils

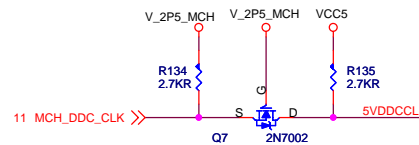
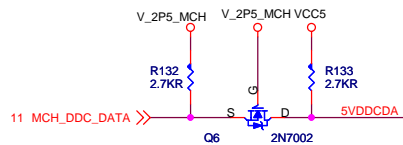
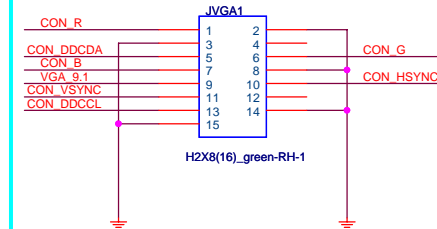
before 150 ohm

12 mils

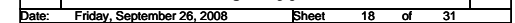
7 mils

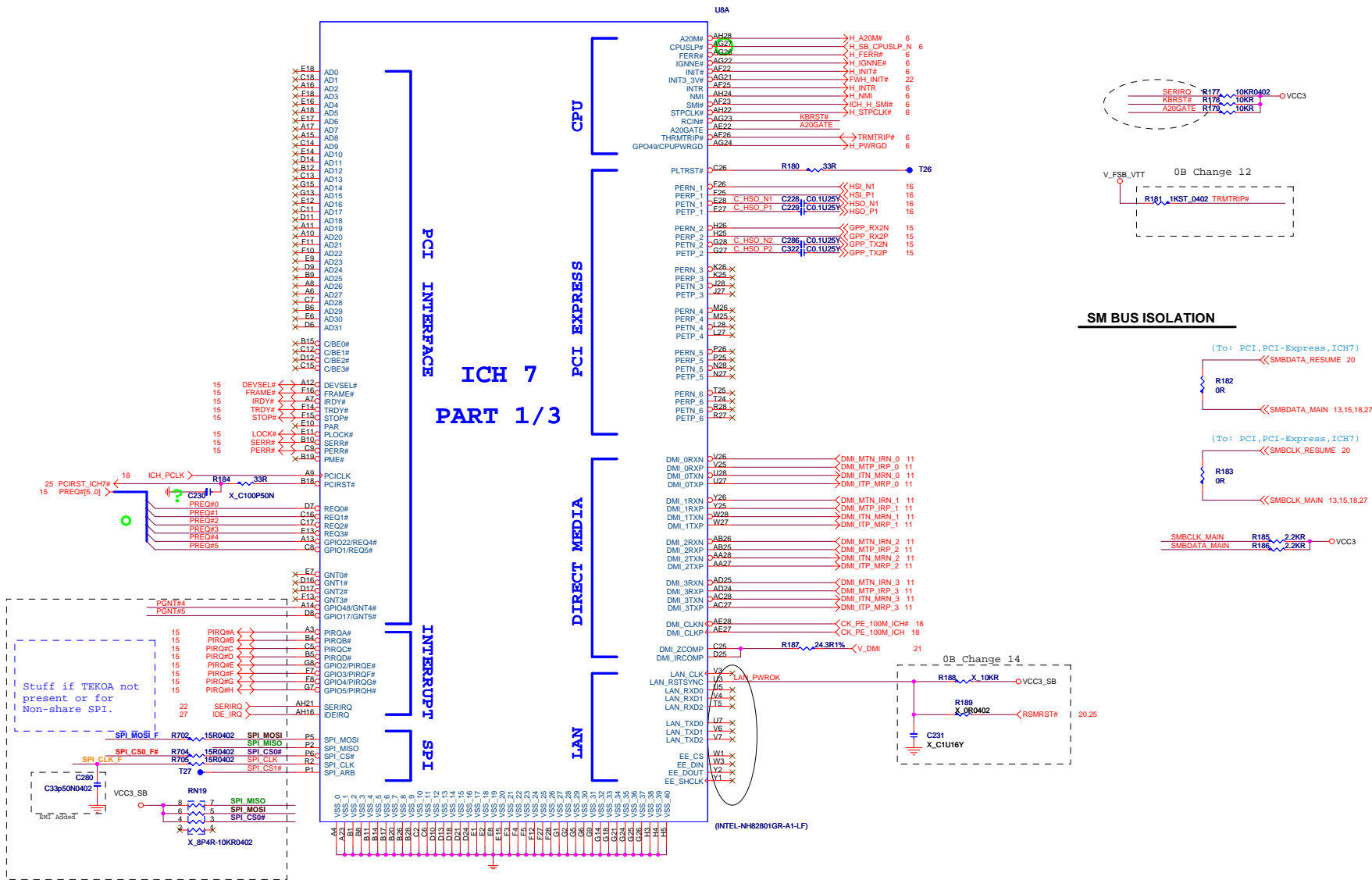


change to 2*8 pin header

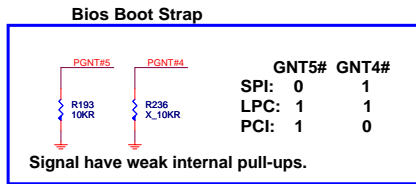
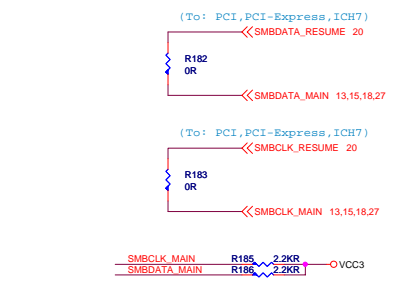


Trace length less than 0.5inches

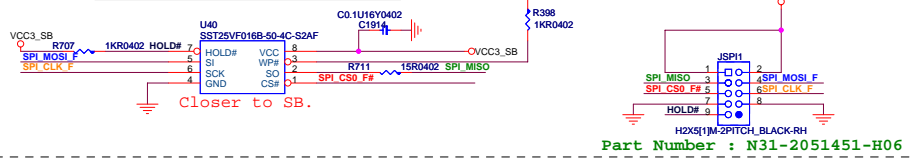




SM BUS ISOLATION



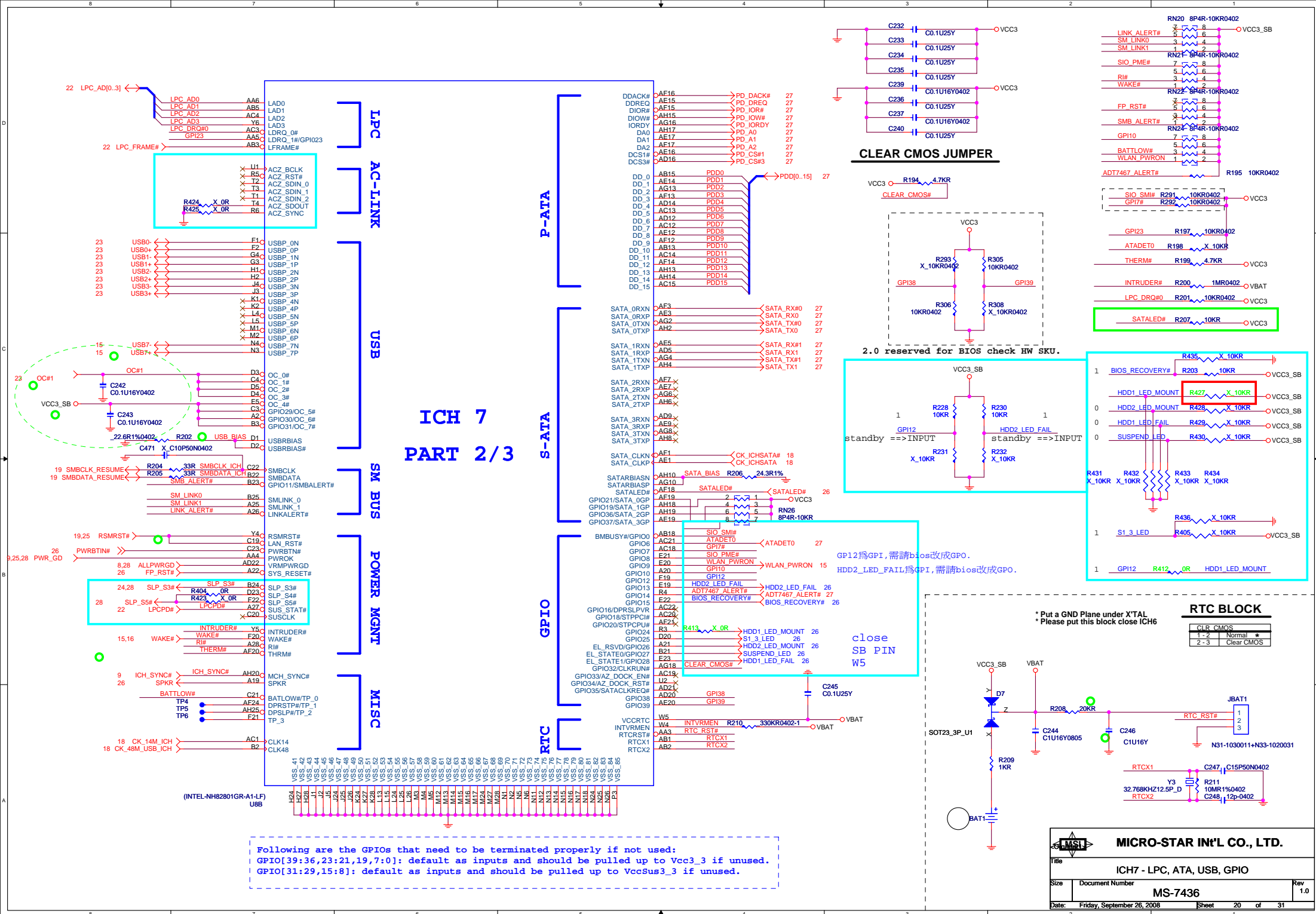
SPI FLASH (8M)

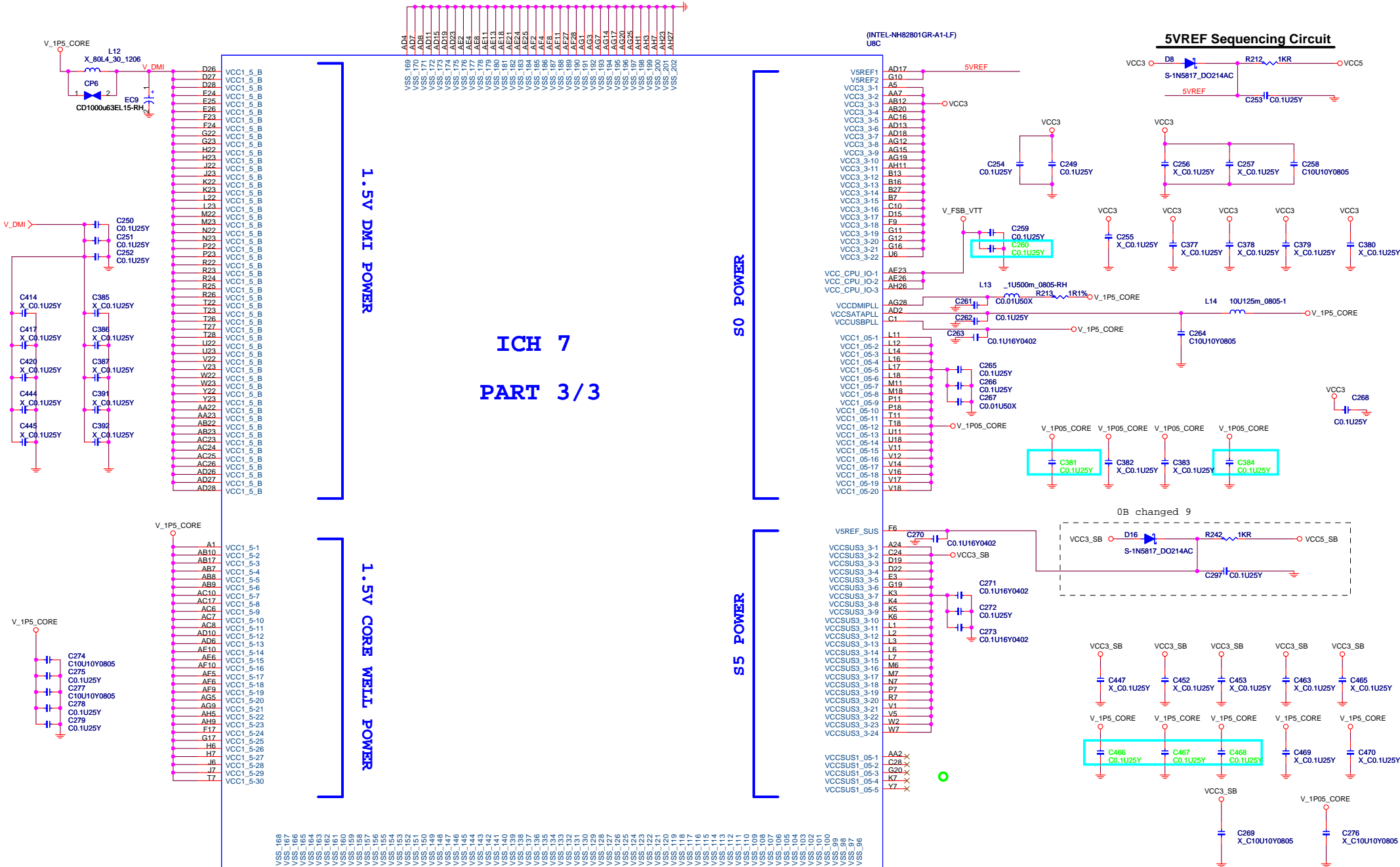


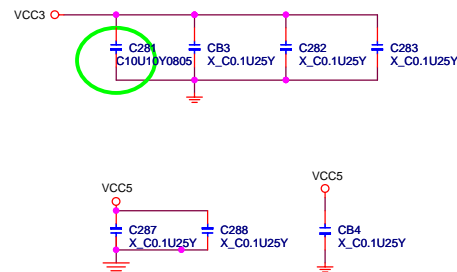
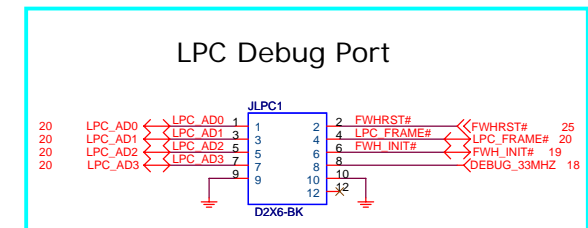
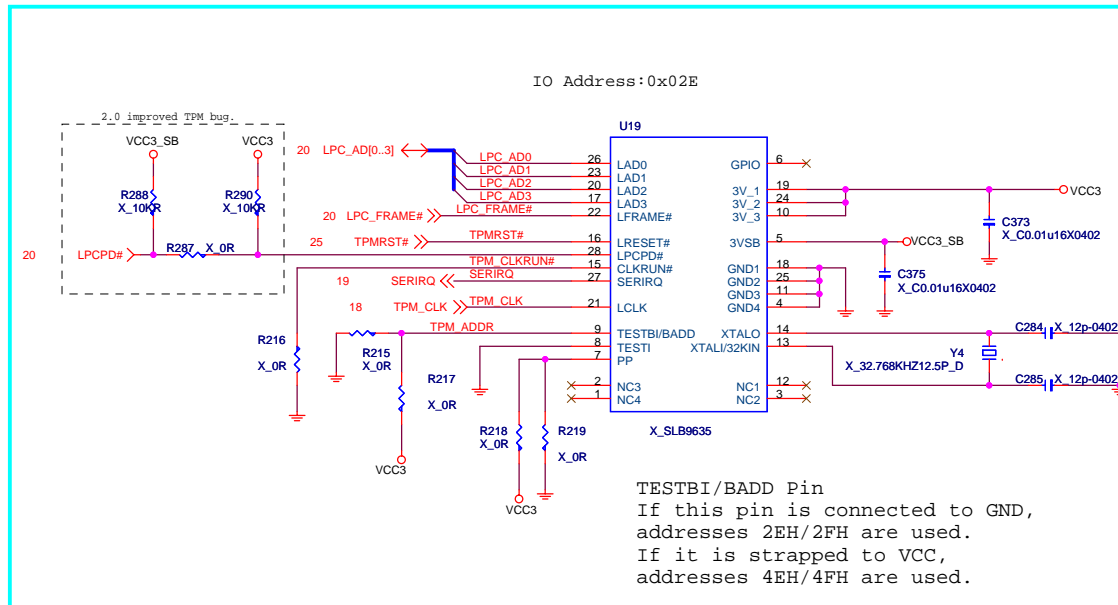
SPI DEBUG PROT

Place close to SPI ROM

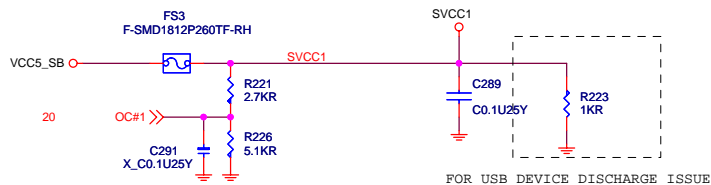
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Title ICH7 - PCI, DMI, CPU, IRQ	
Size	Document Number MS-7436
Date: Friday, September 26, 2008	Sheet 19 of 31





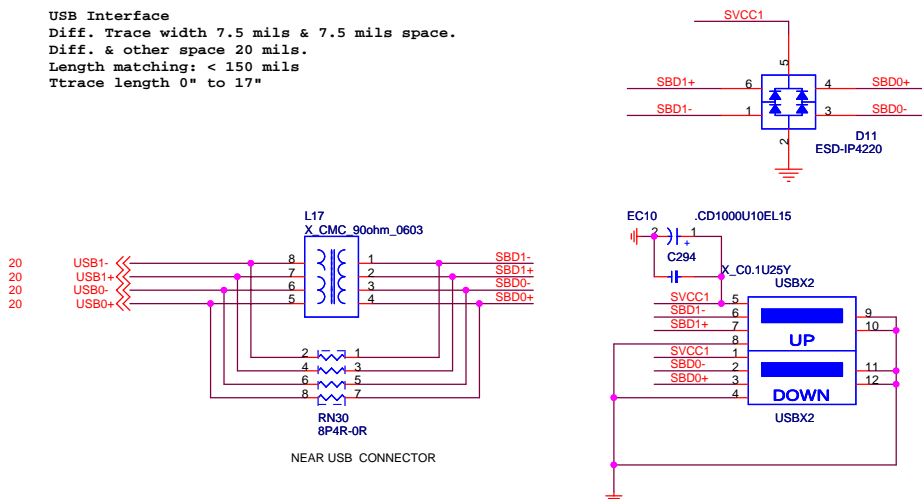


POWER CIRCUIT FOR USB PORT 0,1 (REAR)



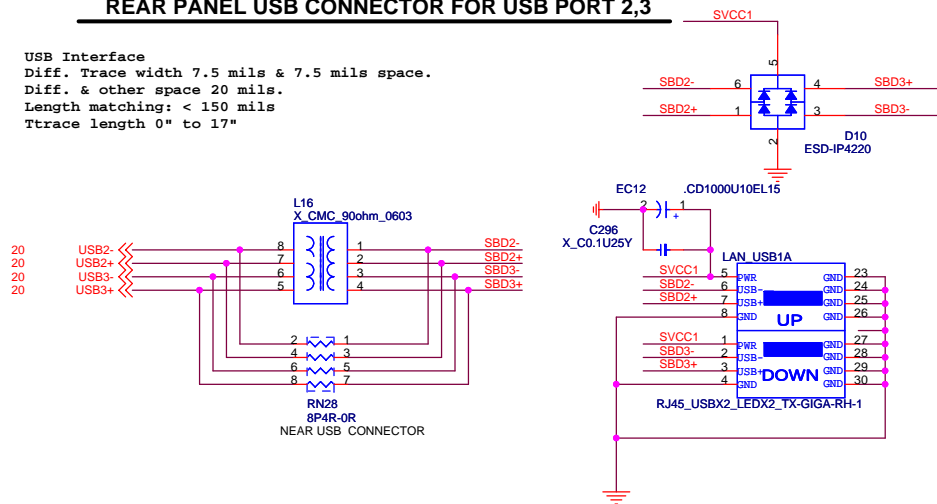
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

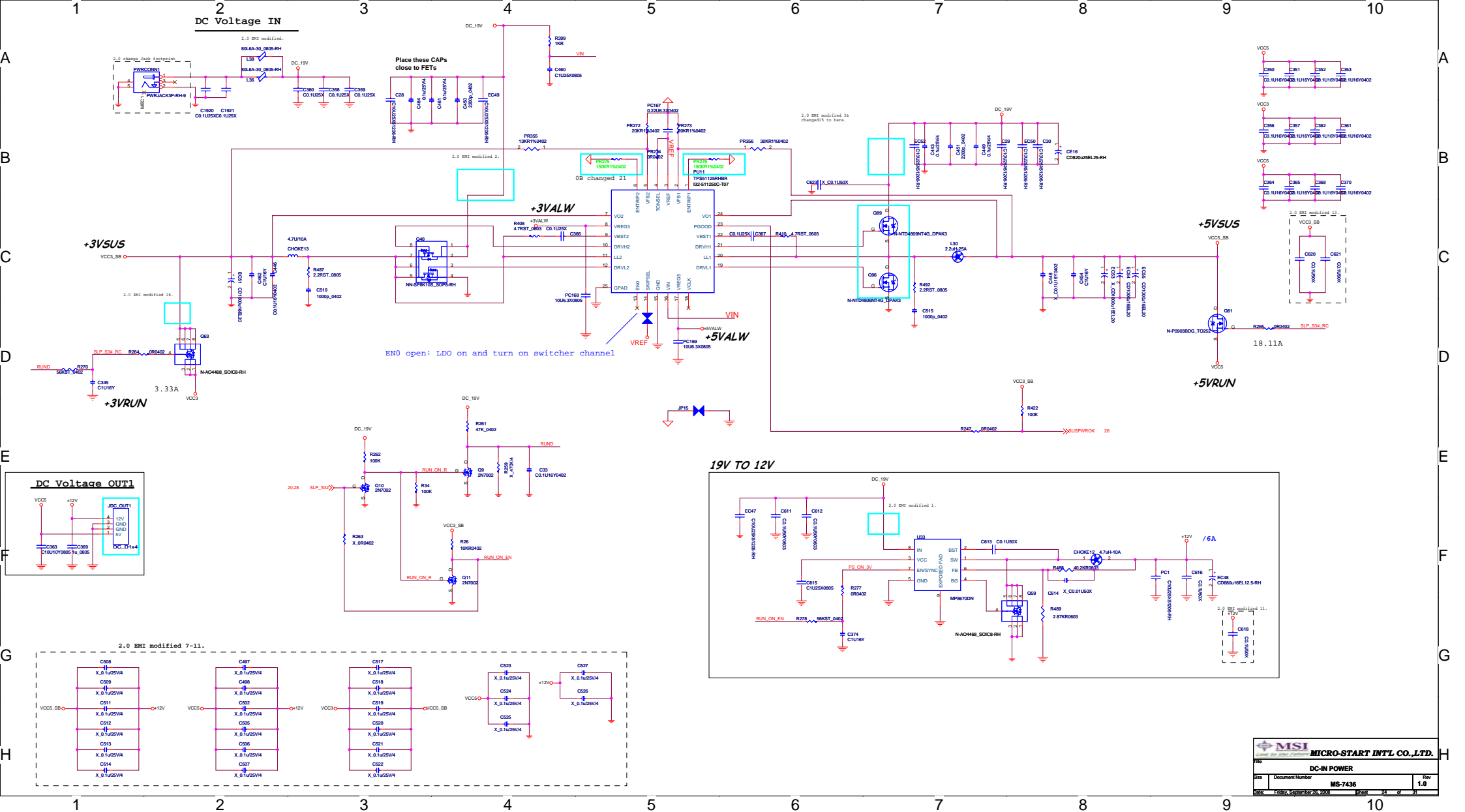
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

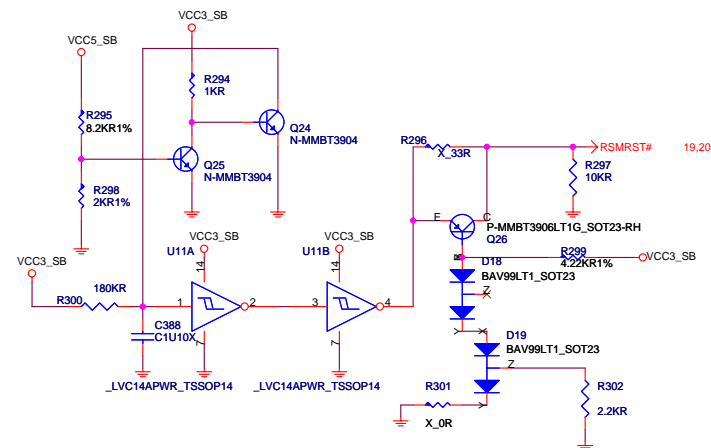
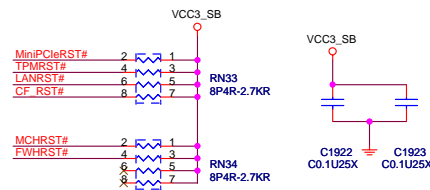
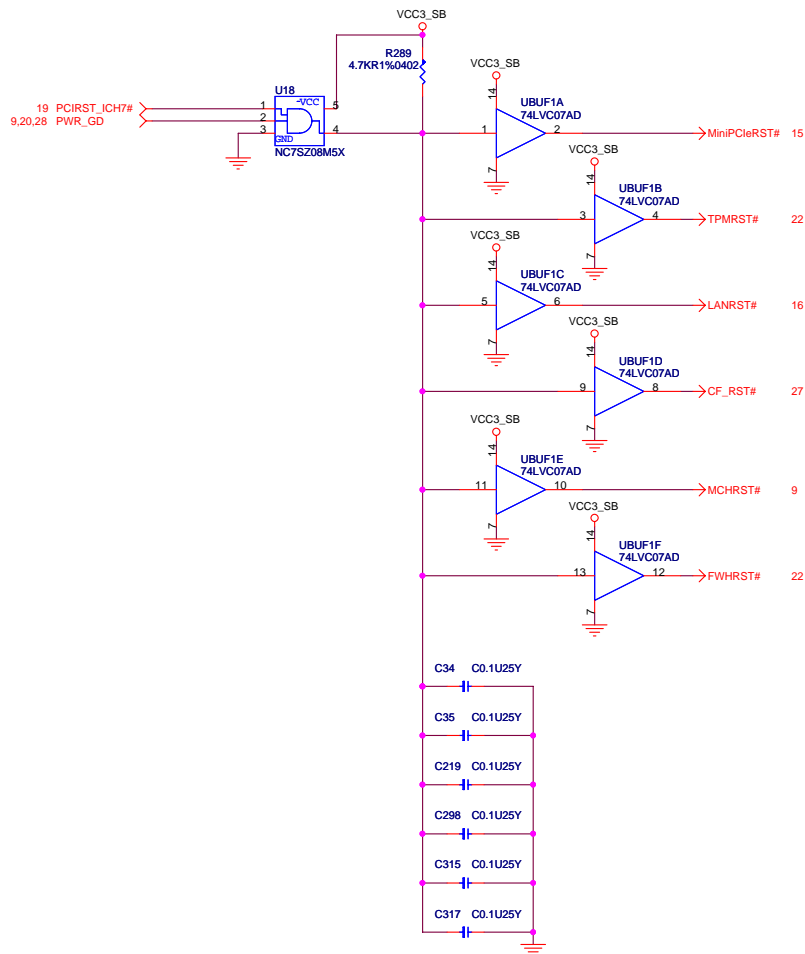


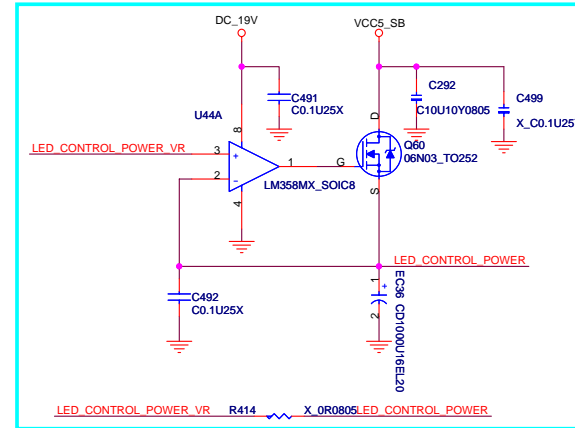
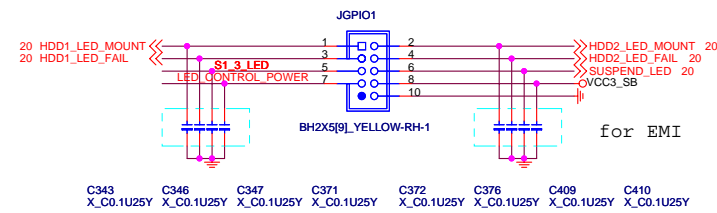
REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

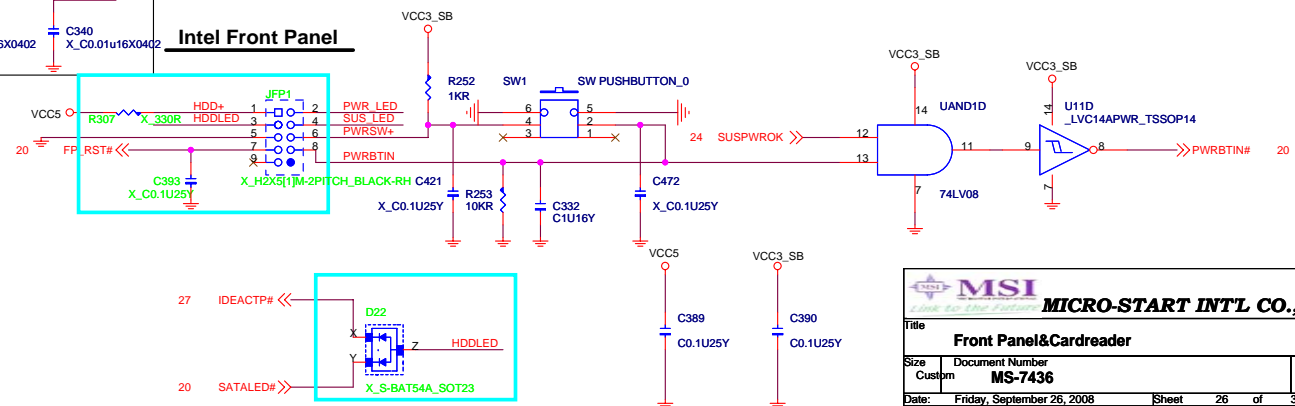
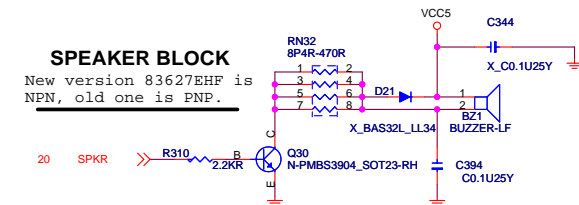




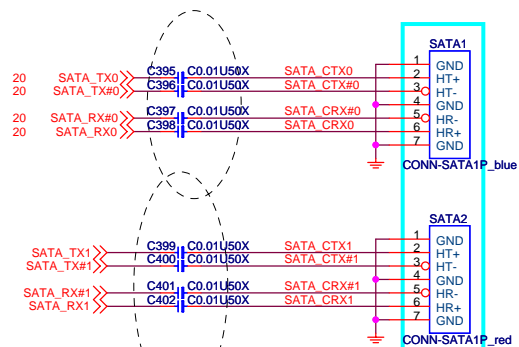




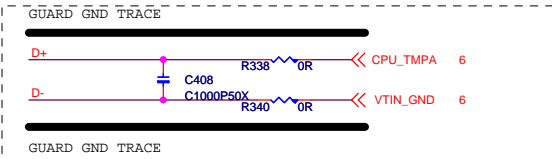
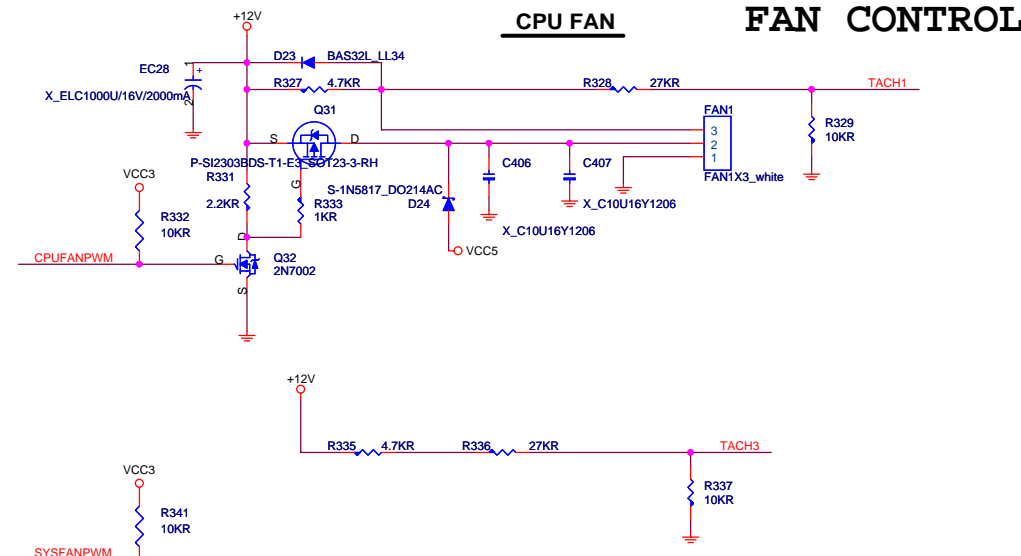
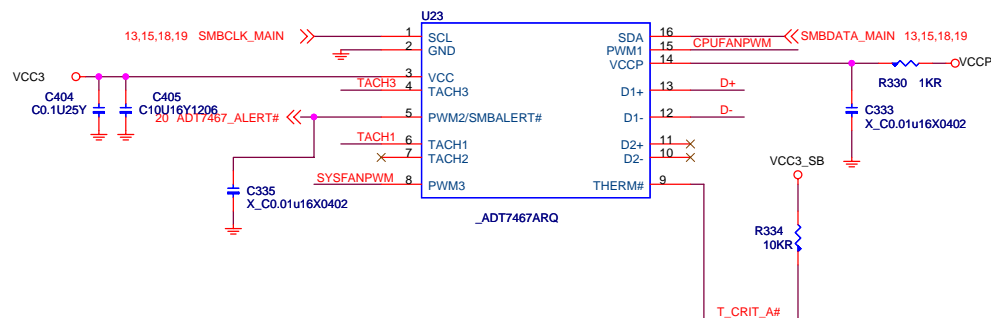
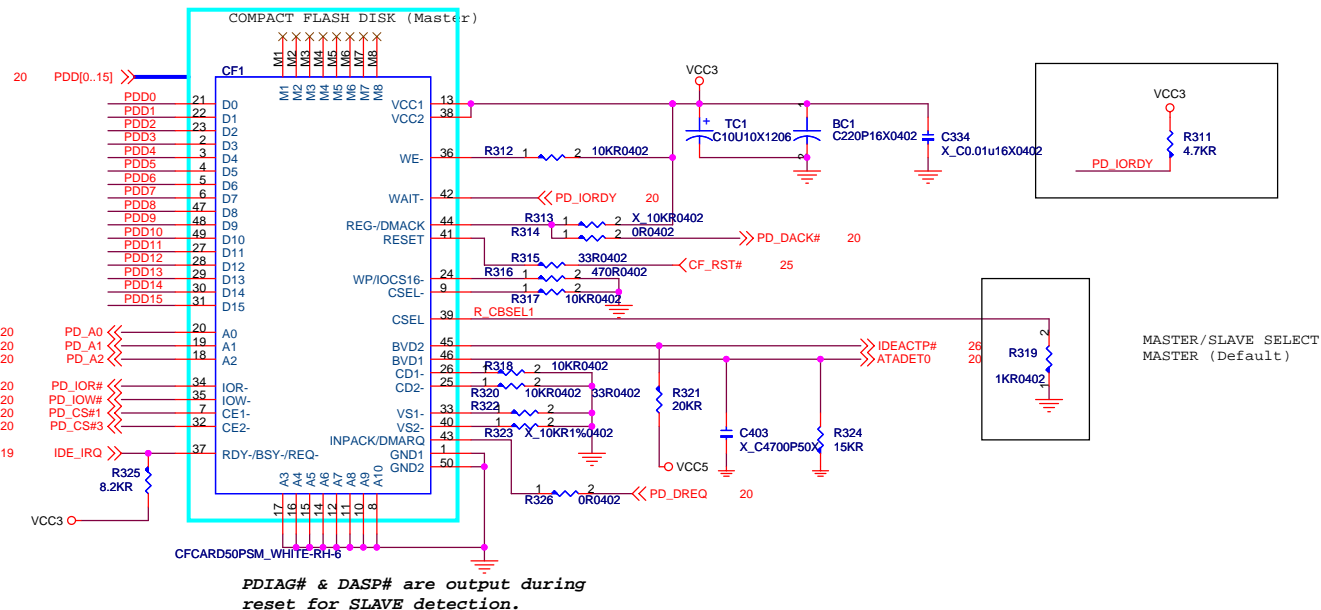
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0



SERIAL ATA CONNECTOR BLOCK



COMPACT FLASH CONNECTOR



PLACE ADT7467 AS CLOSE AS POSSIBLE TO CPU
GUARD TRACE & D+/D- WIDTH:SPACE= 10:10 MIL(MIN)

ACPI Controller

DDR2 1.8V POWER...7.95A

Internal reference $V_{fb}=0.6V$ (+/- 1.5%)
Better than external reference (+/-5%)
==>Using Stand-alone mode

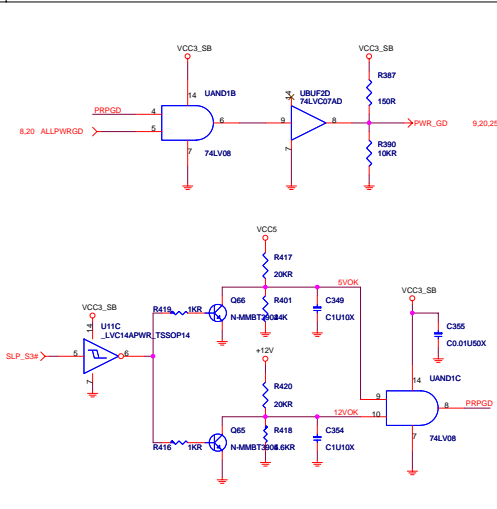
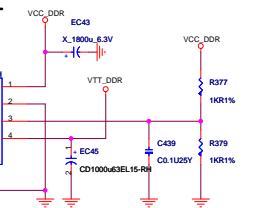
$$V_{fb}=V_{output}*[1.5/(1.5+3.01)]=0.6V \quad V_{output}=1.804V$$

V_1P5_CORE POWER...22.84A

$$V_{fb}=V_{output}*[2/(2+3.01)]=0.6V \quad V_{output}=1.503V$$

VTT1.1V POWER...4.9A

DDR VTT Power

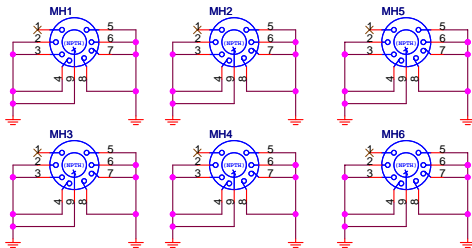


MICRO-STAR INT'L CO., LTD.

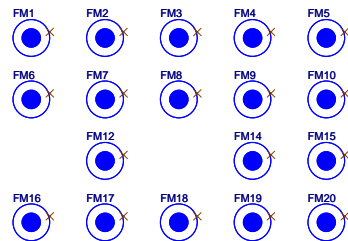
MS7 ACPI CONTROLLER		
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Auto-BOM Manual Parts

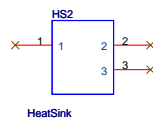
Mounting Holes



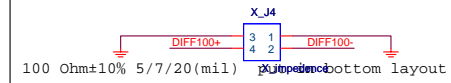
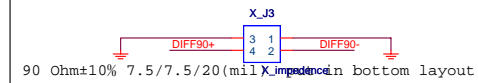
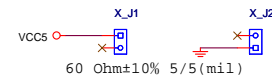
Optics Orientation Holes



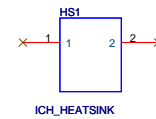
CPU HEAT SINK NB HEAT SINK



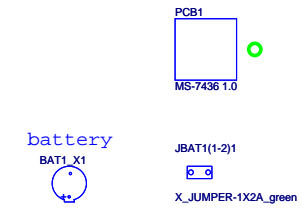
Simulation



SB HEAT SINK



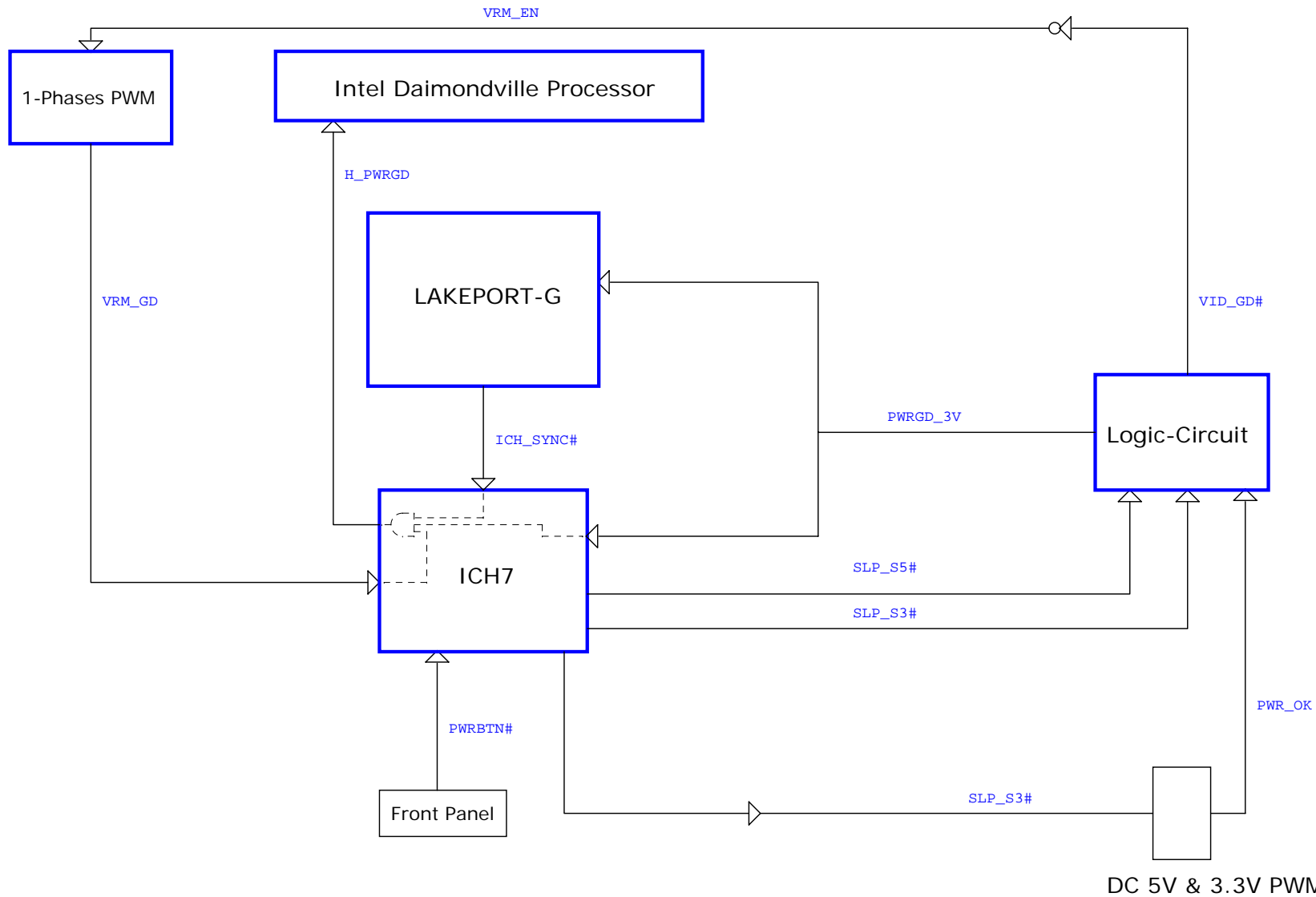
MANUAL PART



MICRO-STAR INT'L CO., LTD.

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PWROK MAP



0A CHANGE 1.0

- 1.page 20 R427,R413不上件,R412上件,解LED BOARD燈號ISSUE.
- 2.page 26 R339 上件100ohm,可解VR調整數率太快.
- 3.page 24 Q89,Q96更換HIGH,LOW SIDE零件,可耐電壓30V,POWER TEAM 建議.
- 4.page 24 remove L39,L40,L41,L42,L43,L44,L45直接連接 解電壓不穩問題.
- 5.page 26 change VR 解無法高溫過錫爐.
- 6.page 26 ADD 調整LED亮度線路.
- 7.page 17 change VGA connector for debug.
- 8.page 27 change sata connector for philips request.
- 9.page 22 tpm 不上件 for philips request.
- 10.page 22 J3002 更名為JLPC1.
- 11.page 28 change EC34 & EC35 from 1000uF EL to 470uF soild cap 解電容高度卡件問題.
- 12.page 26 預留R414以防LED亮度線路不能動作.
- 13.page 13 change so-dimm connector改善製程原料號先(N13-2000370-K06)改到AVL.
- 14.page 26 D TYPE週邊零件不上件.
- 15.Vcore
 - 1. R42: 28.7k ohm (RC)
 - 2. R45: 649 ohm (OCP: 8A)
- VCC3
 - 1. PR275: 130k ohm (OCP: 7A)
- VCC5
 - 1. PR276: 180k ohm (OCP: 28A)
- VCC_DDR
 - 1. R355: 10k ohm (OCP)
- V_1P5_CORE
 - 1. C428: 0.1uF (comp)
 - 2. R367: 10k ohm (OCP)
- 16.page 8 change R30 to 20K & C13 to 10U 解S3 issue .
- 17.add C260,C381,C384,C466,C467,C468 解sa電壓issue.